TECHNICAL INFORMATION

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Stealth Dicing Technology and Applications

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1. Introduction

Stealth dicing process has now evolved to a practical level that makes it the next generation in dicing technology. Stealth dicing offers the following advantages over conventional dicing methods.

- · High-speed dicing
- · High quality (no chips & dust-free)
- · Superior breakage strength (ultra-thin chips)
- · Low kerf loss (better chip production yield)
- · Completely dry process
- · Low running costs

Stealth dicing was initially developed for use in high-speed and high-quality dicing of ultra-thin semiconductor wafers. However, the remarkable advantages stated above are expanding its application range to normal thickness, ultra-fast low-k device wafers and MEMS device wafers.

This document explains the basic principle, mechanism, and typical applications of stealth dicing technology that has been accelerating the practical use.

2. Stealth dicing technology - basic theory and mechanism

2.1 Overview of stealth dicing technology

Fig. 1 shows the basic principle of stealth technology.

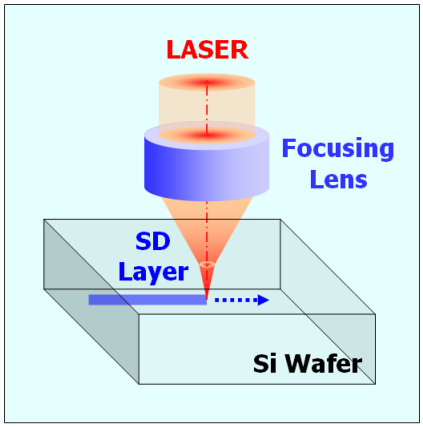


Fig. 1: Basic principle of stealth technology

A laser beam at a wavelength capable of transmitting through a semiconductor wafer is condensed by an objective lens and focused onto a point inside that semiconductor wafer. This laser beam consists of short pulses oscillating at a high repetition rate and can be highly condensed up to a diffraction threshold level. This localized beam is formed at an extremely high peak power density both time and spatially compressed in the vicinity of the light focus point.

When the laser beam transmitting through the semiconductor wafer exceeds a peak power density during the condensing process, a nonlinear absorption effect causes a phenomenon in which extremely high absorption occurs at localized points.

By optimizing the laser and optical system characteristics to cause the nonlinear absorption effect just in the vicinity of the focal point inside the semiconductor wafer, only localized points in the wafer can be selectively laser-machined without damaging the front and back surfaces inside semiconductor wafer.

The semiconductor wafer can be diced by using a stage or similar mechanism that moves the relative positions of the laser beam and wafer in order to scan the wafer at high speeds according to the desired dicing pattern.

Fig. 2 shows spectral transmittance characteristics[1)] of a monocrystalline silicon wafer not doped with any impurities, measured at a room temperature environment.

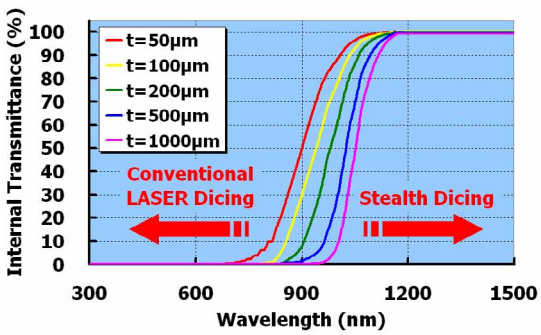


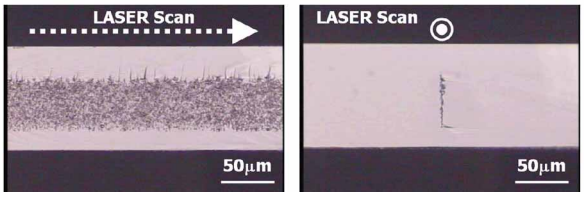
Fig. 2: Spectral transmittance in monocrystalline silicon wafer

This graph shows the pure spectral transmittance characteristics within the wafer, aside from the reflection loss effects on the front and back wafer surfaces.

Though greatly dependent on wafer specifications (thickness and impurity elements and their concentration), monocrystalline silicon wafers generally absorb light at wavelengths shorter than 1,000 nm (nanometers) including the visible to ultraviolet range, yet tend to allow light at longer wavelengths in the near-infrared range to transmit through them. Various laser dicing methods have been investigated on monocrystalline silicon wafers having these optical characteristics. Conventional methods for dicing semiconductor wafers such as monocrystalline silicon mainly utilize the physical phenomena known as heat melt cutting, ablation, and thermal stress cutting, which are caused in the semiconductor wafer when laser energy is greatly absorbed from the surface irradiated by the laser. Most conventional laser dicing methods use laser light at wavelengths that can be highly absorbed by the materials to be diced. These methods therefore have significant problems such as heat and debris that are unavoidably produced during laser machining. This causes adverse effects on device characteristics and reliability. On the other hand, stealth dicing makes use of wavelengths that transmit through the monocrystalline silicon semiconductor wafer to be diced, so that the laser beam can be guided to the vicinity of the focal point inside the wafer, allowing selective, localized laser machining within the wafer. Stealth dicing in this way avoids damaging the wafer surface layers where the actual devices

are formed. This eliminates the problems of conventional laser dicing by ablation, such as thermal effects on the active area, debris contamination, and a drop in breakage resistance due to micro-cracks occurring on the chip edges, which all badly effect device reliability.

Fig. 3 shows results from microscopic observation of the end surface of a 100 µm thick silicon wafer sample actually separated by stealth dicing. Fig. 3 (a) is the cross section of the sample separated by stealth dicing in the direction of the laser scan (dotted line with arrow in the concept view in Fig. 1), while Fig. 3 (b) is the end surface of the sample cleaved and sliced perpendicular to the laser scan before being separated. A stealth dicing layer (SD layer) of a few µm width and having a 40 µm thick is formed in the center section along the thickness direction of the 100 µm thick sample. A perpendicular crack can be observed, running from the top and bottom ends of the SD layer towards the front and back surfaces of the chip. How the chip will separate depends greatly on the extent that this perpendicular crack develops towards the front and back surfaces of the chip. Stealth dicing works by stress-cutting the material from the "inside" and so is fundamentally different from conventional laser dicing methods that cut the material from the "outside".



(a) Laser scan surface (b) Perpendicular to laser scan

Fig. 3: Microscopic observation of stealth dicing sample

2.2 Stealth dicing mechanism

To determine the qualitative state of the SD layer, a 100 µm thick silicon chip separated by stealth dicing was cleaved and sliced as shown in Fig. 4, and the SD layer's crystalline state was evaluated by observing it with a TEM (transmission electron microscope).

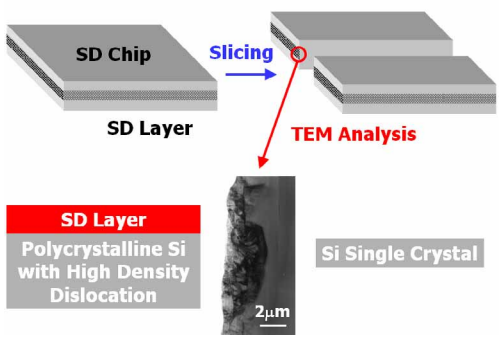
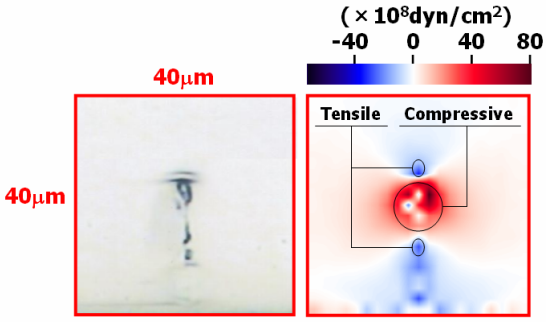


Fig. 4: Evaluation of SD layer crystalline state by TEM

TEM observation proves that the SD layer crystalline state was changed to polycrystalline silicon with high density dislocation, which was confirmed to be a few µm.

The development of the perpendicular cracks facing the front and back surfaces of the chip from the top and bottom ends of the SD layer of Fig. 3 (b) is extremely essential to the chip separation mechanism. Using a 100 µm thick silicon chip sample that was cleaved and sliced in the direction perpendicular to the laser scan, we analyzed the stress distribution over the SD layer and its periphery in a non-separated state by means of Raman spectroscopy. Its evaluation results are shown in Fig. 5.



(a) Optical microscope observation (b) Stress distribution analysis results

Fig. 5: Stress distribution analysis by Raman spectroscopy

A 40×40 µm area around the SD layer shown in (a) was analyzed by Raman spectroscopy. Mapping data on the stress distribution was then acquired from the Raman shift as shown in (b). On this mapping data, a compressive stress is indicated by + values, and a tensile stress indicated by – values, which are acting on the wafer. The darker the color, the more powerful the stress generated in the wafer.

It can be seen that an extremely powerful compressive stress is generated in the SD layer where a polycrystalline silicon state with high density dislocation was observed by TEM as shown in Fig. 4. An extremely powerful tensile stress can also be seen at the top and bottom of that SD layer. The volumetric expansion that accompanies the localized polycrystallization of the SD layer is assumed to generate this powerful compressive stress. If a spherical SD layer were formed, the stress distribution in the peripheral area would show the compressive stress gradually reducing towards the periphery away from the SD layer. However, probably due to the fact that the SD layer is formed with an extremely high aspect ratio, the very powerful tensile stress is concentrated at the top and bottom of the SD layer.

The perpendicular cracks developing towards the chip front and back surfaces from the top and bottom of the SD layer region, as shown in Fig. 3 (b), are originated from the high density dislocation region where an extremely powerful compressive stress is locally generated. These cracks are easily prone to develop towards the front and back surfaces of the chip due to the very powerful tensile stress generated at the top and bottom ends of the SD

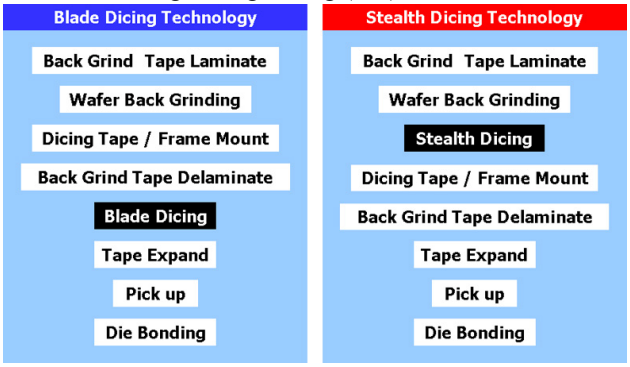
layer. This facilitates the chip separation by using an external force such as tape expansion described later on.

The above description covers the basic principle and mechanism of stealth dicing.

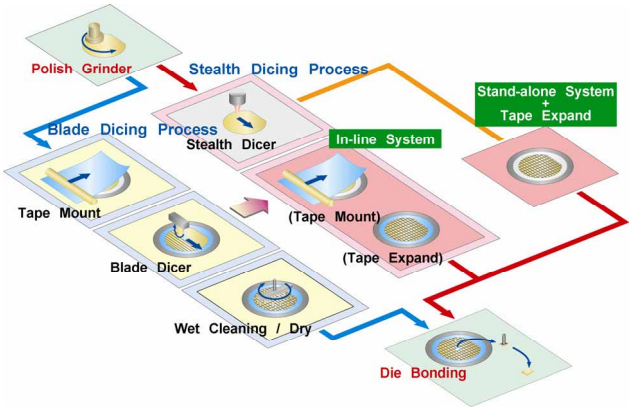
3. Application of stealth dicing technology

3.1 Application of stealth dicing

Fig. 6 shows the comparison between actual processes in stealth dicing (SD) and conventional blade dicing (BD) used in a back-end process of ultra-thin semiconductor wafers involving back grinding (BG).



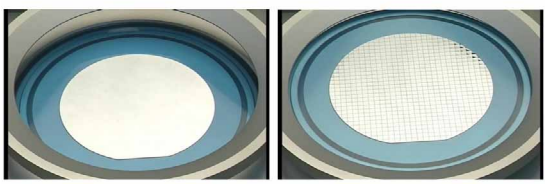
(a) BD method (b) SD method



(c) Process Flow

Fig. 6: Comparison of actual processes

In the SD method, stealth dicing is performed from the ground back surface after the back grinding (BG) process. In contrast to conventional dicing where the chips are completely separated during blade dicing (BD), the SD method allows the individual chips to be still integrated with the wafer even after stealth dicing. The stealth-diced chips are separated afterwards by tape expansion. Fig. 7 shows the state of the chips before and after tape expansion that separates the chips.

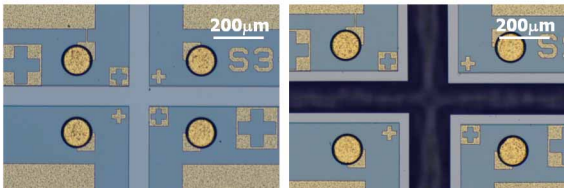


(a) Before tape expansion (b) After tape expansion

Fig. 7: Chip separation by tape expansion

Fig. 7 shows a 6-inch 100 µm thick wafer that was stealth-diced and then separated by tape expansion into 5×5 mm size chips.

Although the ease of chip separation can be controlled by the stealth dicing conditions, individual chips are basically separated by utilizing a force generated during tape expansion that acts to expand the space between the chips. Fig. 8 shows the state of the so-called "street intersections" between the chips on the stealth-diced device wafer both before and after tape expansion.



(a) Before expansion (b) After expansion

Fig. 8: Device sample before and after tape expansion

As can be seen from Fig. 8 (a), no change appears after stealth dicing and prior to tape expansion. (This is the reason that this dicing method was named "stealth dicing".) As the tape gradually expands, the wafer is separated into the desired small chip shape conforming to the SD layer pattern formed within the wafer, as shown in Fig. 8 (a). The area in the shape of a black cross in Fig. 8 (b) shows the new kerf formed by tape expansion.

Chip separation by tape expansion in stealth dicing can be performed by the tape expanding process used in conventional dicing method. The number of processing steps in stealth dicing is therefore the same as in conventional dicing. On the other hand, unlike the cutting process by a mechanical blade in conventional method, stealth dicing works by a non-contact process using laser scanning so the process speed can be drastically improved.

Fig. 9 shows the process speed and process quality of the BD and SD methods.

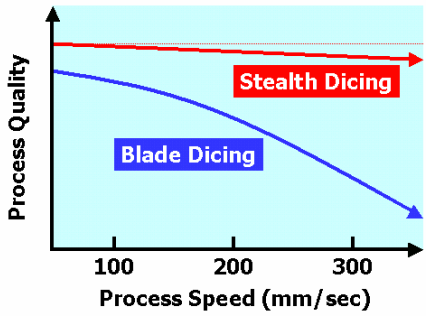


Fig. 9: Process speed and process quality

Here, the process quality indicates the external appearance quality of separated chips.

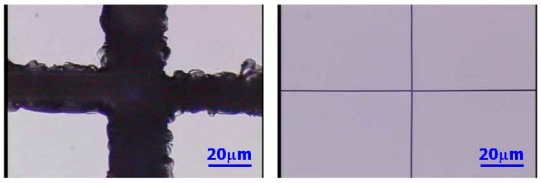
Using higher process speeds in blade dicing tends to cause a drastic drop in the process quality. In the SD method, on the other hand, the process speed does not greatly affect the process quality, so an extremely high process quality can be maintained.

This tendency that the process speed affects the process quality becomes drastically larger as the wafer to be diced becomes thinner. This means the SD method offers tremendous advantages when manufacturing ultra-thin devices.

3.2 Evaluation of stealth dicing process quality

The process quality in the BD and SD methods is compared next using an actually processed sample.

The photographs in Fig. 10 show examples comparing the process quality on the front side edge of a chip diced from a 100 μm thick silicon sample. These show microscopic images in the vicinity of the dicing street intersection near the chip surface. Fig. 10 (a) shows results from the BD method at a process speed of 100 mm/sec. Fig. 10 (b) shows results from the SD method at a process speed of 300 mm/sec.

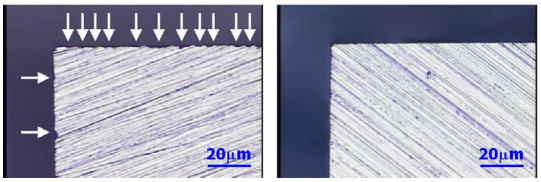


(a) BD method (b) SD method

Fig. 10: Comparison of process quality on wafer surface

In the BD method in Fig. 10 (a), kerf loss occurs that is basically equivalent to the blade width, and chipping and cracks occur at levels from a few to 10 μm on the chip edge. In the SD method in Fig. 10 (b), the process speed is 3 times faster than the BD method yet no chipping or cracks occur. These results confirm the qualitative comparison of process speed and process quality shown in Fig. 9.

Fig. 11 shows a comparison of process quality on the backside edge of a 50 μm thick silicon wafer sample (backside BG #2000), made by microscopic observation in the vicinity of the chip backside edge. Fig. 11 (a) is the result by an improved BD method, and (b) is by the SD method.



(a) Improved BD method (b) SD method

Fig. 11: Comparison of process quality on back side

The improved BD method in Fig. 11 (a) is different from the conventional BD method because it utilizes a method[2] that delivers superior backside edge quality. The improved BD method improves quality by reducing the backside chipping. However, it is still fundamentally a mechanical cutting technique and therefore damages the layers on the chip end surface due to contact from the dicing blade the same as when back-grinding a surface. Moreover, chipping occurs on the backside edge on a level of several μm as shown by the arrows in Fig. 11 (a). In the SD method, on the other hand, absolutely no chipping has occurred, as can be seen from Fig. 11 (b).

During actual dicing on devices of 100 μm or less, this type of chipping is a major cause that lowers the breakage resistance like a damage layer on the BG surface does. Taking some kind of countermeasure in subsequent stress relief processes is necessary in order to maintain chip breakage strength at a level where significant damage will not occur during handling. It is therefore extremely essential to suppress backside edge chipping.

Fig. 12 shows results from a three-point bend test[3] on the improved BD and SD chip samples shown in Fig. 11.

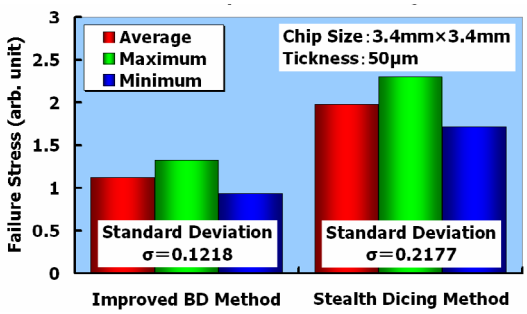


Fig. 12: Comparison of breakage strength

The back surface of the samples were finished by BG#2000 as shown in Fig. 11. To reduce the BG#2000 effects, this test was performed by evaluating a chip sample that was extracted from a specified position on a wafer where the longitudinal direction of the load indenter for the three-point load test was always perpendicular to the cutting marks on the back surface. The test showed that the SD method had high average, maximum, and minimum values for breakage strength compared to the improved BD method. These results reflect the chipping state of the chip backside edge shown in Fig. 11.

4. Applications of SD technology

4.1 Applying SD technology to DAF

Stealth dicing technology can be applied to DAF (Die Attach Film) as described in the following example. When the thickness of wafers to be diced is thin, DAF is utilized in the chip mounting process after the dicing process shown in Fig. 6. The DAF functions as an adhesive when stacking and pasting thin chips at a high mounting density.

In the actual process, DAF mount is made immediately after stealth dicing shown in Fig. 6. The super-thin wafer on which the DAF is mounted is then diced. In the conventional BD method, this dicing is basically the mechanical cutting operation so that simultaneous, high quality cutting (dicing) of the silicon wafer and DAF is extremely difficult because they are different in mechanical characteristics. Peels and folds often occur in the DAF material and the device characteristics and reliability are

affected. In the SD method, on the other hand, DAF is mounted on the wafer that has already been stealth-diced, and then the frame and tape are mounted and BG tape peeled off. In the next step of tape expansion to separate the chips, DAF is also separated into a shape identical to the size of each silicon chip.

Fig. 13 shows microscopic images of a chip attached with DAF film after separation into chips by tape expansion. These microscopic images of the chip end surface, front side and back side (tape side) clearly show that there is no DAF delamination or protrusion and the separation is sharp with contours the same as the chip shape. Because the adhesion strength between the DAF and wafer and between the DAF and tape is extremely high, and also because the chip clearance equivalent to the kerf width is "0" before tape expansion, a high quality DAF separation can also be made in the same shape as the chip during the tape expansion. In conventional blade dicing, a kerf width equal to the blade width is an unavoidable factor, so it is difficult to use the same DAF separation mechanism.

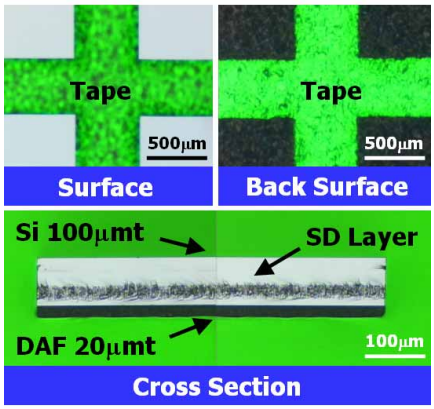


Fig. 13: Stealth-diced sample with DAF attached

4.2 Applying stealth dicing to low-k devices

As already described, the conventional BD method is basically a mechanical cutting process. This makes the BD method difficult to use for high quality dicing of composite materials made up of different elements.

Practical use of low-k materials for high-speed devices are being accelerated in order to lower the dielectric constant of interlayer insulating films with the intended goal of higher speed device operation. However, the low-k material itself has extremely low mechanical strength and is easily damaged by external stress. Producing high quality chips with the conventional BD method is very difficult. Moreover, along with lowering the dielectric constant of low-k materials, some materials make dry process a prerequisite, so the number of problems that cannot be solved by the BD method is increasing.

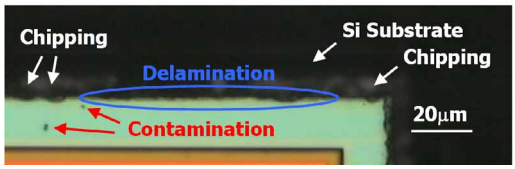
Recently, intensive efforts are being made to deal with these circumstances by developing practical, non-contact dicing technology that uses lasers on low-k devices[4]. This is achieved by various methods. However, they all use a common technique that makes the laser beam be efficiently absorbed by the silicon and low-k materials, to utilize a physical phenomenon called "laser ablation" for wafer dicing.

Fig. 14 shows microscopic observations of the dicing process quality when the laser ablation method and SD method are used on a low-k device.

Fig. 14 (a) shows results of dicing when laser ablation is performed with a pulsed UV laser. On the edges of the sample made into chips by laser ablation, chipping and delamination of the low-k multilayer film are observed due to the effects of heat. Debris contamination can also be found on the periphery. These types of chipping and delamination of the low-k multilayer film and debris contamination have serious affects on device characteristics and reliability and so are the most significant problems that must be resolved.

In contrast, when using the SD method, there were none of the chipping, delamination and debris contamination those were found in the laser ablation method and the high quality dicing was confirmed.

The distances from the device pattern to the chip edge are different in Fig. 14 (a) and Fig. 14 (b) when the device pattern is used as a reference standard. This difference in distance shows that kerf loss is occurring due to laser ablation the same as in the BD method.



(a) Laser ablation method

(b) SD method

Fig. 14: Comparison of low-k device dicing

The image for the SD method shows nearly a stress-cutting process near the front and back surfaces with a kerf loss close to nearly "0". However, the laser ablation method generates machining dust in amounts equivalent to the kerf loss. So methods to collect and remove this dust have to be considered. As the chip size in the process grows smaller, the kerf loss has more significant effects on the chip production yield per wafer. Reducing this kerf loss becomes a critical problem when dealing with ultra-small chip devices.

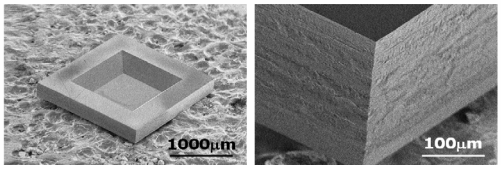
4.3 Applying stealth dicing to MEMS

The MEMS (Micro Electro Mechanical System) field has grown rapidly in recent years as a new frontier in semiconductor technology[5]. MEMS devices formed as 3-dimensional structures in various shape on a silicon substrate have appeared and continuously create new product value in the semiconductor industry.

Producing creative and innovative MEMS devices requires solving the problems of dicing processes already in use.

A dry process is ideal due to the properties of MEMS devices. These MEMS devices are also extremely sensitive to external impacts, so applying the BD method is basically impossible and makes some kind of technological innovation necessary. This situation has drastically spurred market demand for stealth dicing of MEMS related devices. One application of stealth dicing to MEMS devices is the MEMS chip sensor device. Fig. 15 shows SEM (scanning electron microscope) images of the SD process performed on the MEMS chip sensor device.

Fig. 15 (a) shows the overall MEMS device with a chip size of 2×2 mm and a thickness of 300 µm. A hollow with a depth of several µm is created in the center of the chip, and the actual device is formed on the opposite side of the chip.



(a) Overall chip (b) Enlarged section of edge periphery

Fig. 15: SEM observation of SD-processed MEMS chip

In this type of sample, the ultra-thin sections in the center of the chip are easily damaged by external impacts from the blade and cleaning water during dicing by the conventional BD method. The BD method is therefore impossible to use on this type of sample.

Fig. 15 (b) shows an enlarged image of the periphery of the closer edge section of Fig. 15 (a). No chipping or cracks have occurred and an extremely sharp edge can be seen. The SD layer can also be observed on the end surface.

5. Effects of stealth dicing technology on device characteristics

To qualitatively evaluate the effect of stealth dicing technology on device characteristics, device electrical characteristics were tested using a photodiode test pattern shown in Fig. 16.

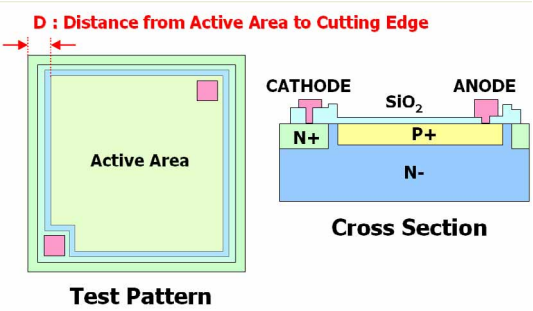


Fig. 16: Photodiode test pattern

Dark current versus reverse voltage characteristics of photodiodes processed by the BD and SD methods were measured. The results are compared in Fig. 17 using the distance D from the photodiode active area to the chip edge (distance D in Fig. 16, D=20, 50, 30 µm) as the parameter.

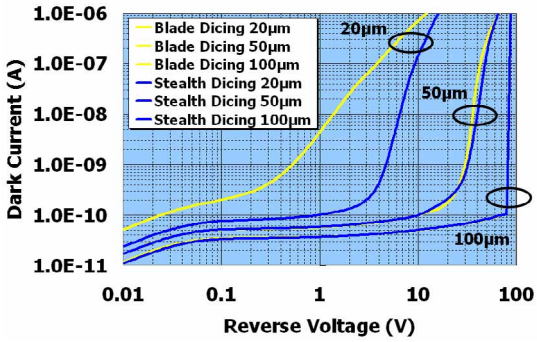


Fig. 17: Dark current vs. reverse voltage of photodiodes

Both the SD and BD methods show a trend for the breakdown voltage (reverse voltage at which dark current increases suddenly) to lower as the D value becomes smaller. However, a significant difference occurs between the SD and BD methods when D=20 µm. This evaluation of characteristics depends on the device itself. However, it shows that the SD method affects device characteristics within a narrow range compared to the BD method and that the distance from the end of the device to the chip edge can be shortened even further.

6. Conclusion

This technical document describes the basic principle, mechanism and some applications of stealth dicing technology. In stealth dicing, a laser beam at a wavelength capable of transmitting through the material is condensed on an internal point in that material This selectively forms a mechanical damage layer (stress layer) in a localized point near the light focus area so that the material is cut from the "inside". The operating principle of stealth dicing is fundamentally different from conventional blade dicing technology that cuts the material from the "outside". Stealth dicing therefore has the potential to overcome problems with dicing that have been difficult to solve up to now. Current work is centering on practical technology for dicing silicon semiconductor wafers. We refined and put together major elements of stealth technology to develop an "SD engine", which is a laser module integrated with optical systems. This module is currently supplied to Tokyo Seimitsu with whom we have formed a business tie-up. In a joint effort with TOKYO SEIMITSU CO., LTD. we have developed the MAHOHDICING MACHINE (See Fig. 18) to a practical level and placed the first machines on the market.

Fig. 18: MAHOHDICING MACHINE

The huge potential offered by stealth dicing technology is leading to its rapid expansion into materials besides silicon wafers. Stealth dicing can be applied to other materials including compound semiconductors, glass, and sapphire, etc. We are currently developing a new "SD engine" to meet needs in these other market areas. We are also drawing up specific planning aimed at expanding our operational range to swiftly respond to market needs.

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